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DESCRIPTION

VIDEO COMPOSITION CIRCUIT

TECHNICAL FIELD

The present invention relates to a video composition circuit such as a television and, more particularly, to a reduction in the circuit scale.

BACKGROUND ART

Conventionally, when image composition or filtering is carried out in a video composition circuit such as a television, different circuits are prepared every time composition is carried out.

Hereinafter, a conventional video composition circuit will be described.

Figure 3 shows a conventional video composition circuit.

In figure 3, 301 denotes an external storage unit provided outside the video composition circuit, 302 denotes a transfer control unit for controlling transfer of data from the external storage unit 301, 303 denotes an internal storage unit provided in the video composition circuit, 304 denotes an OSD output unit for processing OSD display data outputted from the internal storage unit 303 to perform OSD output, 305 denotes a sub video output unit for processing sub video data outputted from the

internal storage unit 303 to perform sub video output, 306 denotes a main video output unit for processing main video data outputted from the internal storage unit 303 to perform main video output, and 307 denotes a video output unit for combining the outputs from the OSD output unit 304, the sub video output unit 305, and the main video output unit 306 to perform video output. Further, 308 denotes, for example, a display having a digital signal input, which displays the video signal outputted from the video output unit 307. In the above-mentioned construction, the constituents other than the external storage unit 301 and the display 303 are fabricated on the same chip.

Further, an LUT (Look Up Table) circuit for performing color conversion processing such as CLUT (Color Look Up Table) processing and gamma correction processing is incorporated in the OSD output unit, and a DDA (Digital Differential Analysis) circuit for performing inter-pixel interpolation by digital differential analysis is incorporated in each of the main video output unit 306 and the sub video output unit 305 according to need, and further, a DDA circuit and two α composition circuits are incorporated in the main video output unit 306.

The operation of the video composition circuit constructed as described above will be described with reference to figure 4.

The main video, the sub video, and the OSD data are serially and successively outputted from the external storage unit 301, respectively.

During a main video 1 transfer period 403, main video data 408 is transferred from the external storage unit 301 through the transfer control unit 302 to the internal storage unit 303, and stored as main video 1 (411) in the internal storage unit 303. Subsequently, during a main video 2 transfer period 404, another main video data 408 is transferred from the external storage unit 301 through the transfer control unit 302 to the internal storage unit 303, and further, the main video data 408 is transferred to the main video output unit 306 and processed, and stored as data 412 after main video filtering in the internal storage circuit 303.

Next, during a sub video transfer period 405, sub video data 409 is transferred from the external storage unit 301 through the transfer control unit 302 to the internal storage unit 303, and further, the sub video data 409 is transferred to the sub video output unit 305 and processed, and the processed main video and sub video data 413 is stored in the internal storage circuit 303.

Next, during an OSD transfer period 406, OSD display data 410 is transferred from the external storage unit 301 through the transfer control unit 302 to the internal storage unit 303, and further, the OSD display data 410 is transferred to the OSD output unit 304 and processed. Furthermore, in the subsequent-stage video output unit 307, the OSD display data processed by the OSD output unit 304 and the previously processed main video and sub video data 413 are combined, thereby obtaining final

output data 414.

In the operation of the above-mentioned circuit, the processings are finally carried out in synchronization with a display period 402 which is a display speed of frames based on a horizontal sync signal 401.

Patent Document 1: Japanese Published Patent Application No. Hei.11-352946 (Page 17, Figure 1)

DISCLOSURE OF THE INVENTION

In the conventional video composition circuit, the complicated video output unit 307 for α-blending three outputs from the OSD output unit 304, the sub video output unit 305, and the main video output unit 306 is required. Further, since the data of the respective layers, i.e., the OSD display data, the sub video data, and the main video data, are stored in the internal storage unit 303, the size of the internal storage unit is undesirably increased. Further, both of the main video output unit 306 and the sub video output unit 305 are provided with the DDA (Digital Differential Analysis) circuits, and thereby the size of the whole device is undesirably increased. Further, the OSD output unit, the sub video output unit, and the main video output unit are specially incorporated, and therefore, it is difficult to alter the functions of these circuits.

The present invention is made to solve the above-described problems and has for its object to provide a video composition

circuit that can reduce the circuit scale.

In order to solve the above-mentioned problems, according to Claim 1 of the present invention, there is provided a video composition circuit for receiving plural pieces of video data which are successively inputted in serial order, performing a predetermined video processing for predetermined video data, and combining plural pieces of video data to output composite data, and the video composition circuit comprises: a video processing unit to which plural pieces of video data are successively inputted in serial order, performing a predetermined video processing to the inputted video data, and outputting the processed video data; a video data composition unit for combining the plural pieces of video data outputted from the video processing circuit to output composite data; and a data storage unit for holding the video data outputted from the video data composition unit; and the video data composition unit combining the video data read from the data storage unit and the video data outputted from the video processing circuit, as well as combining the plural pieces of video data outputted from the video processing circuit.

According to Claim 2 of the present invention, in the video composition circuit defined in Claim 1, the video processing unit, the data storage unit, and the video data composition unit are constituted on the same chip.

According to Claim 3 of the present invention, in the video

composition circuit defined in Claim 1, the plural pieces of video data successively inputted in serial order are main video, sub video, and OSD video which is additional information to be displayed simultaneously with the main and sub videos; and the video data composition unit is a circuit having an α-blending function.

According to Claim 4 of the present invention, the video composition circuit defined in Claim 3 further includes an external storage unit for holding the plural pieces of video data that are successively inputted in serial order, the external storage unit being placed outside the chip; and the video data composition unit reads the video data outputted from the external storage unit and the α-blended video data which is stored in the data storage unit in the chip, and subjects these data to α-blending again.

According to Claim 5 of the present invention, in the video composition circuit defined in Claim 3, the video data composition unit having the α-blending function reads the video data outputted from the external storage unit, and the α-blended video data which is stored in the data storage unit in the chip, and subjects these data to vertical filtering.

According to Claim 6 of the present invention, in the video composition circuit defined in Claim 1, the video data composition unit writes the video data which is obtained as a result of combining the video data read from the data storage

unit and the video data outputted from the video processing unit, over the video data which has previously been stored in the data storage unit.

As described above, according to Claim 1 of the present invention, there is provided a video composition circuit for receiving plural pieces of video data which are successively inputted in serial order, performing a predetermined video processing for predetermined video data, and combining plural pieces of video data to output composite data, and the video composition circuit comprises: a video processing unit to which plural pieces of video data are successively inputted in serial order, performing a predetermined video processing to the inputted video data, and outputting the processed video data; a video data composition unit for combining the plural pieces of video data outputted from the video processing circuit to output composite data; and a data storage unit for holding the video data outputted from the video data composition unit; and the video data composition unit combining the video data read from the data storage unit and the video data outputted from the video processing circuit, as well as combining the plural pieces of video data outputted from the video processing circuit. Therefore, the circuit scale can be reduced by integrating the video processing unit, the video data composition unit, and the data storage unit on a single circuit.

According to Claim 2 of the present invention, in the video

composition circuit defined in Claim 1, the video processing unit, the data storage unit, and the video data composition unit are constituted on the same chip. Therefore the circuit scale can be reduced.

According to Claim 3 of the present invention, in the video composition circuit defined in Claim 1, the plural pieces of video data successively inputted in serial order are main video, sub video, and OSD video which is additional information to be displayed simultaneously with the main and sub videos; and the video data composition unit is a circuit having an α-blending function. Therefore, there is required only one α-blending circuit having an OSD display function, a sub video display function, a main video display function, and an α-blending function, whereby the circuit scale can be reduced. Further, since the OSD output unit, the sub video output unit, and the main video output unit are united to be one circuit, functions which have conventionally been realized for sub video but have not been realized for OSD can be used for OSD.

According to Claim 4 of the present invention, the video composition circuit defined in Claim 3 further includes an external storage unit for holding the plural pieces of video data that are successively inputted in serial order, the external storage unit being placed outside the chip; and the video data composition unit reads the video data outputted from the external storage unit and the α-blended video data which is stored in the

data storage unit in the chip, and subjects these data to α-blending again. Therefore, the internal storage unit is used so that data are overwritten, whereby the amount of usage of the internal storage unit can be reduced.

According to Claim 5 of the present invention, in the video composition circuit defined in Claim 3, the video data composition unit having the α-blending function reads the video data outputted from the external storage unit, and the α-blended video data which is stored in the data storage unit in the chip, and subjects these data to vertical filtering. Therefore, the internal storage unit is used so that data are overwritten, whereby the amount of usage of the internal storage unit can be reduced.

According to Claim 6 of the present invention, in the video composition circuit defined in Claim 1, the video data composition unit writes the video data which is obtained as a result of combining the video data read from the data storage unit and the video data outputted from the video processing unit, over the video data which has previously been stored in the data storage unit. Therefore, the internal storage unit is used so that data are overwritten, whereby the amount of usage of the internal storage unit can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating the construction of

a video processing apparatus (video composition circuit) according to a first embodiment of the present invention.

Figure 2 is a block diagram illustrating the construction of a video processing circuit included in the video processing apparatus according to the first embodiment of the present invention.

Figure 3 is a block diagram illustrating the construction of a conventional video processing apparatus.

Figure 4 is a diagram for explaining the processing operation of the video processing apparatus according to the first embodiment of the present invention.

Figure 5 is a diagram for explaining the processing operation of the conventional video processing apparatus.

BEST MODE TO EXECUTE THE INVENTION

(Embodiment 1)

Hereinafter, an embodiment of the present invention will be described with reference to figures 1 and 2.

Figure 1 shows a video composition circuit according to a first embodiment of the present invention. In figure 1, reference numeral 101 denotes an external storage unit for holding main video data, sub video data, and OSD display data, which is provided outside the video composition circuit. Reference numeral 104 denotes an internal storage unit for holding the main video data, the sub video data, and the OSD

display data, which is provided inside the video composition circuit. Reference numeral 102 denotes a transfer control unit for controlling transfer of data from the external storage unit 101 to the internal storage unit 104, and reference numeral 103 denotes a video processing circuit which receives the video data read from the external storage unit 101 by the transfer control unit 102, and the video data read from the internal storage unit 104, and subjects these video data to video processing. Reference numeral 105 denotes, for example, a display having a digital signal input, for displaying data outputted from the video processing circuit 103. In the above-mentioned construction, the transfer control unit 102, the video processing circuit 103, and the internal storage unit 104 are fabricated on the same chip (LSI).

Hereinafter, the operation of the video composition circuit constructed as described above will be described with reference to figure 4.

Initially, during a main video 1 transfer period 403, main video 1 data stored in the external storage unit 101 is transferred through the transfer control unit 102, processed in the video processing circuit 103, and stored in the internal storage unit 104 as main video 1 data 411. Next, during a main video 2 transfer period 404, main video 2 data stored in the external storage unit 101 is transferred through the transfer control unit 102, processed in the video processing circuit 103,

and written over the data 411 to be stored as main video filtered data 412 in the internal storage unit 104.

Next, during a sub video transfer period 405, sub video data stored in the external storage unit 101 is transferred through the transfer control unit 102, and processed in the video processing circuit 103 together with the data (412) which has previously been stored in the internal storage unit 104, and the processed data is written over the data 412 to be stored as main video + sub video data 413 in the internal storage unit 104.

Next, during an OSD transfer period 406, OSD data stored in the external storage unit 101 is transferred through the transfer control unit 102, and processed in the video processing circuit 103 together with the data 413 which has previously been stored in the internal storage unit 104, and the processed data is written over the data 413 to be stored as output video 414 in the internal storage unit 104.

Figure 2 shows the specific construction of the video processing circuit 103. In figure 2, reference numeral 201 denotes an external storage access request circuit which outputs an external storage request signal 202 that requests an access to the external storage unit 101, and an external storage read address 203 that indicates a read address thereof, through the transfer control unit 102 to the external storage unit 101. Thereby, external storage read data 204 is obtained from the external storage unit 101 through the transfer control unit 102.

Further, the external storage access request circuit 201 outputs a request signal 205 that requests an access to the internal storage unit 104, to an internal storage read interface (hereinafter referred to as I/F) 206.

The internal storage read I/F 206 receives the request signal 205, and outputs an internal storage read address 207 to the internal storage unit 104. Thereby, read data 208 is obtained from the internal storage unit 104.

A parallel/serial conversion circuit 209 converts the output 208 from the internal storage read I/F 206, from parallel data to serial data, and outputs a video output 210 to the internal storage unit 104.

The internal storage unit 104 outputs the video output converted into serial data to the outside as an output of the video composition circuit.

A selector 211 selects either the external storage read data 204 that is read by the external storage access request circuit 201 or the read data 208 that is read by the internal storage read I/F 206.

A shift circuit 212 processes the read data selected by the selector 211 into pixel-unit data as required.

A DDA (Digital Differential Analysis) circuit 214 performs inter-pixel interpolation by digital differential analysis as required, thereby performing scale-up and scale-down of the video data outputted from the shift circuit 212 in the horizontal

direction.

A shift circuit 213 processes the read data 208 outputted from the internal storage read I/F 206 into pixel-unit data as required.

A LUT (Look Up Table) circuit 215 performs color conversion processing such as CLUT (Color Look Up Table) processing and gamma correction processing as required.

The CLUT processing is a processing to convert video data that is expressed by a color number such as OSD display data into color data on the basis of a CLUT. The gamma correction processing is also performed using a LUT for gamma correction.

An α-blending circuit 216 performs α-blending of the output of the DDA circuit 214 and the output of the LUT 215. The α-blending is a processing to blend images on the basis of α information expressing a transparency. While in this embodiment images are blended on the basis of predetermined α information, images to be blended themselves may have α information.

An internal storage write I/F 217 writes write data 219 which is obtained as a result of blending by the α-blending circuit 216, into the internal storage unit 104 according to an internal storage write address 218.

A processor 220 controls the operations of the respective units in the video processing circuit 103.

Hereinafter, a description will be given of the operation of the video processing circuit 103 constituted as described above.

Initially, the processor 220 gives a command to the external storage access request circuit 201, and an external storage request signal 202 and an external storage read address 203 are transmitted to the transfer control unit 102. Then, the external storage read data 204 is returned from the transfer control unit 102. Simultaneously, a request signal 205 is transmitted to the internal storage read I/F 206, and an internal storage read address 207 is issued in timing with the request signal 205. When the internal storage read address 207 is issued, read data 208 is returned from the internal storage unit 104 to the internal storage read I/F 206. The returned data is transferred to the shift circuit 213, and processed into dot-unit data as required. The processed data is transferred to the LUT circuit 215, and subjected to color conversion processing such as CLUT (Color Look Up Table) processing and gamma correction processing as required.

On the other hand, the external storage read data 204 is transmitted through the external storage access request circuit 201 and the selector circuit 211 to the shift circuit 212, and processed into dot-unit data as required. The processed data is transmitted through the DDA (Digital Differential Analysis) circuit 214 and subjected to scaling up or scaling down in the horizontal direction. The output of the DDA circuit 214 and the output of the LUT circuit 215 are subjected to α-blending in the α-blending circuit 216. A result of the α-blending is input to

the internal storage write I/F 217, and the processing result is written in the internal storage unit 104 according to the internal storage write address 218 and the internal storage write data 219.

The above-mentioned α-blending circuit 216 is also able to perform, in addition to α-blending, vertical filtering by reading horizontal two lines on the same screen. For example, each of two lines of main video is read as an input of the α-blending and processed by the α-blending circuit 216, whereby vertical filtering can be carried out.

Further, when processing two kinds of data stored in the internal storage unit 104, a read timing is given to the internal storage read I/F 206 by the processor 220, and an internal storage read address 207 is given to the internal storage unit 104. Thereby, the read data 208 is returned from the internal storage unit 104, and two kinds of data from the internal storage unit 104 are read into the internal storage read I/F 206. One of the two kinds of data is transferred through the selector circuit 211 to the shift circuit 212, and processed into dot-unit data as required, and then the processed data is transferred through the DDA circuit to be subjected to scaling up or scaling down in the horizontal direction. The other data is transferred to the shift circuit 213, and processed into dot-unit data as required, and then transferred to the LUT circuit 215 to be subjected to CLUT processing or gamma correction as required. The output of the

DDA circuit 214 and the output of the LUT circuit 215 are input to the α-blending circuit 216 to be α-blended. The α-blended data is transferred to the internal storage write I/F 217, and then transferred to the internal storage unit 104 according to the internal storage write address 218 and the internal storage write data 219. When the data stored in the internal storage unit 104 is processed and the data before the processing is not required, the data after the processing is written over the data before the processing, thereby reducing the capacity of the internal storage unit that is needed in this video composition circuit.

Finally, the final output data stored in the internal storage unit 104 is transferred through the read data 208 to the internal storage read I/F 206 using the internal storage read address 207. The transferred data is transferred to a parallel-serial conversion circuit 209 to be output as video output 210.

In the video composition circuit according to the first embodiment, video composition processing for combining the data of the external storage unit 101 and the data of the internal storage unit 104 is carried out using the video processing circuit 103 having the OSD display function, the sub-video display function, the main-video display function, and the α-blending function, and writing of the processing result into the internal storage unit 104 is repeated. Therefore, it is required to provide only one α-blending circuit having the OSD display

function, the sub-video display function, the main-video display function, and the α-blending function, resulting in a reduction in the circuit scale. Further, since the OSD output unit, the sub-video output unit, and the main-video output unit are united to be one circuit, it is possible to realize processings such as scaling up and scaling down which have been realized for sub-video but have not been realized for OSD. Further, since overwriting of data is carried out as mentioned above, the amount of usage of the internal storage unit can be further reduced. Moreover, since vertical filtering for the data in the external storage unit and the data in the internal storage unit is carried out using the α-blending function of the video processing circuit, whereby the α-blending circuit can be operated as a vertical filter circuit, resulting in a further reduction in the circuit scale.

Further, since the video composition circuit needs to have only one DDA circuit and one α-blending circuit in contrast to the conventional circuit, the number of these circuits can be reduced by half, resulting in a further reduction in the circuit scale.

APPLICABILITY IN INDUSTRY

In a video processing apparatus according to the present invention, a video processing unit, a video data composition unit, and a data storage unit are integrated as one circuit, whereby

the circuit scale is reduced, resulting in a minimized apparatus.